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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,520	04/15/2004	Ron Nevo	18189	9085

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TYCO TECHNOLOGY RESOURCES
4550 NEW LINDEN HILL ROAD, SUITE 140
WILMINGTON, DE 19808-2952

EXAMINER	
CALEY, MICHAEL H	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,520	NEVO ET AL.	
	Examiner	Art Unit	
	Michael H. Caley	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima et al. (U.S. Patent No. 5,596,665 "Kurashima") in view of Sampson et al. (U.S. Patent No. 4,767,179).

Regarding claim 1, Kurashima discloses a method for assembling an opto-electric module (Figure 1 element 1) comprising:

at least one OSA (Figure 2 elements 2 and 5) having an optical axis (Column 11 lines 35-37), an optical end (Figure 2 element 10a), an electrical end (Figure 2 side of element 11a), and an electrical interface (Figure 2 side of element 11a) at said electrical end, a circuit board (Figure 2 element 8) having electrical contacts (Figure 2 element 46b), and a connector interface (Figure 20 elements 9 and 22) cooperating with the OSA such than an optical connector (Figure 20 element 9) is optically coupled to the OSA, the method comprising:

providing an assembly (Figure 2 element 7) comprising the connector interface and a substrate (Figure 2 element 15) having a cavity for receiving the OSA, the cavity being aligned with the connector interface (Figure 8 element 22,

Figure 20) such that, when the OSA is disposed in the cavity, the OSA is positioned to optically couple with a mating connector of an optical component connected to the connector interface (Figure 20 element 9);

placing the circuit board in a particular position relative to the cavity such that, when the OSA is disposed in the cavity, the electrical interface is positioned to electrically couple with contacts on the circuit board (Figure 14);

placing the OSA in the cavity (Figures 5-8); and

electrically connecting the electrical interfaces to the contacts (Figures 13-15).

Kurashima fails to disclose the step of affixing the circuit board to the substrate and also fails to disclose the step of electrically connecting the electrical interface to the contacts as performed after the OSA is disposed in the cavity and the circuit board is fixed to the substrate. Sampson, however, teaches affixing a circuit board (12) to a substrate (22) having a cavity for an OSA (16) and connecting the electrical interface after the OSA is disposed in the cavity and the circuit board is fixed to the substrate (Column 3 lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have affixed the circuit board to the substrate and to have electrically connected to the electrical interface after disposing the OSA and fixing the circuit board in the display device disclosed by Kurashima. One would have been motivated to affix the circuit board and the substrate to maintain their positional relationship within the opto-electric module assembly as taught by Sampson. One would have been motivated to electrically connect the electrical

interface after the OSA is disposed in the cavity and the circuit board is fixed to the substrate to allow for the circuitry to be aligned and therefore allow for the circuitry to be easily connected by soldering (Column 3 lines 1-8).

Regarding claim 2, Kurashima discloses the cavity as dimensioned to receive the OSA snugly so that the position of the OSA is defined in the module (Figures 2, 6, and 8).

Regarding claim 3, Kurashima discloses the substrate as resilient and urges against the OSA when the OSA is placed therein (elements 24A and 24B; Figures 11 and 12).

Regarding claim 4, Kurashima discloses the step of placing the OSA in the cavity as comprising snapping the OSA into the cavity (Column 9 lines 24-50, Column 10 lines 5-31; Figures 11 and 12).

Regarding claim 5, Kurashima discloses the substrate as having a second cavity (Figure 2).

Regarding claim 6, Kurashima discloses a first structure to align the connector interface to the cavity (Figures 2 and 20).

Regarding claim 7, Kurashima fails to disclose a second structure to align the circuit board relative to the cavity. Sampson, however, teaches a second structure to align the circuit board relative to the cavity (element 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second structure on the substrate to align the circuit board relative to the cavity in the display device disclosed by Kurashima. One would have been motivated to affix the circuit board and the substrate to maintain their positional relationship within the opto-electric module assembly in achieving a reliable electrical connection between the opto-electric module and the circuit board.

Regarding claim 9, Kurashima discloses placing the OSA by first inserting the optical end thereof into the connector interface and then placing the electrical end into the cavity such that the electrical interface is urged against the circuit board (Column 9 lines 24-50, Column 10 lines 5-31; Figures 11 and 12).

Regarding claim 10, Kurashima discloses the OSA as placed in the cavity by first inserting the optical end thereof into the connector interface and then placing the electrical end into the cavity such that the electrical interface is urged against the circuit board (Column 11 lines 16-54).

Regarding claim 11, Kurashima discloses the OSA as one of either a receiving OSA or a transmitting OSA (Column 6 lines 45-49).

Regarding claim 12, Kurashima discloses the electrical interface as having electrical leads extending from the OSA essentially parallel to the optical axis of the OSA and a flexible circuit of electrical conductors extending orthogonally from the electrical leads (Figure 2 elements 2 and 47).

Regarding claim 13, Kurashima discloses the circuit board as having a top and bottom orientation when mounted on the substrate, the contacts being disposed on the top of the circuit board, and wherein the OSA is placed in the cavity such that the electrical conductors overlay the contacts (Figures 3 and 4).

Regarding claim 14, Kurashima discloses the conductors as resilient and as biased into the circuit board when the OSA is disposed in the cavity (Column 7 lines 49-63; Figure 3).

Regarding claim 15, Kurashima discloses the flexible circuit as not extending between the electrical leads and the contacts in a straight line (Figure 2).

Regarding claim 16, Kurashima discloses the circuit board as planar and parallel to the optical axis (Figure 2).

Regarding claim 17, Kurashima discloses the flexible circuit as extending orthogonally from the electrical leads and as bending around the circuit board (Figure 2).

Regarding claim 20, Kurashima discloses attaching a cover to the substrate to contain and hold secure the OSA (Figure 2 element 4).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima in view of Sampson and in further view of Ishibashi et al. (U.S. Patent No. 5,596,663 "Ishibashi").

Kurashima as modified by Sampson fails to disclose the second structure as an orifice adapter to receive a pin and the circuit board as comprising an orifice to receive a pin, and wherein affixing the circuit board to the substrate comprises sequentially inserting a pin through an orifice of the circuit board and an orifice through the substrate. Ishibashi, however, teaches such a fixing and alignment structure (circuit board 30, circuit board orifice 31, substrate 10, orifice adapter 11, pin 71).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate such a fixing and alignment structure between the circuit board and the substrate in the display device disclosed by Kurashima. One would have been motivated to include such an alignment structure as a means of automating the assembly process and to allow for the substrate to be easily press-fit onto the circuit board (Column 12 lines 32-48).

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima in view of Sampson and in further view of Gilliland et al. (U.S. Patent No. 6,358,066 "Gilliland").

Kurashima as modified by Sampson fails to disclose the amount of overlap between the contacts and the electrical conductors as adjusted to control impedance after the OSA is placed in the cavity. Gilliland, however, teaches such a feature as a means of matching the impedance of the connection to that of the host device (Column 6 lines 26-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the amount of overlap between the contacts and the electrical conductors to control impedance after the OSA is placed in the cavity. One would have been motivated to match the impedances of the connection and the host device to avoid the cost and inconvenience of additional impedance match equipment and to benefit from an efficient contact between electrical components (Column 1 lines 28-48).

Response to Arguments

Applicant's arguments filed 2/9/06 have been fully considered but they are not persuasive.

Regarding the rejection of claim 1 as unpatentable over Kurashima in view of Sampson, Applicant argues that the process is not obvious because there is no likelihood of success. Applicant argues that the electrical connection between the OSA and the circuit board cannot be made after the OSA and the circuit board are placed in the housing. Applicant further argues that the OSA and the circuit board would not fit into the housing until the two are connected and bent by an angle D shown in Figure 3.

The examiner disagrees with Applicant's conclusion of no likelihood of success. Element 15 of Kurashima has been identified as the substrate having the cavity. The claim

language would only require that the OSA be disposed in the cavity of element 15 before establishing electrical connection. Therefore, it would not have been necessary to insert the OSA and the circuit board into the housing (element 4) before establishing electrical connection. Accordingly, the issue of whether the OSA and circuit board may be inserted into the housing (element 4) before establishing electrical connection is regarded as moot.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael H. Caley whose telephone number is (571) 272-2286. The examiner can normally be reached on M-F 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael H. Caley
April 25, 2005
mhc

ANDREW SCHECHTER
PRIMARY EXAMINER